

ABSTRACT

A video platform architecture for video processing includes complex video compression/decompression algorithms in a computer with a two-dimensional Single-Instruction Multiple-Data (SIMD) array architecture. The video platform architecture includes one or more video processing modules, on-chip shared memory, and a general-purpose RISC central processing unit CPU used as a system controller. Each video processing module includes a rectangular array of processing elements (PEs), a block load/store unit, a global-accumulation unit. Video to be processed is configured into blocks of data, and a general-purpose CPU used as a local controller. A plurality of registers are provided in the processing elements and the block load/store unit to support two-dimensional processing of the data blocks. Types of registers used include block registers, vector registers, scalar registers, and exchange registers. Each of these registers is designed to hold a short ordered one- or two-dimensional set of video data (data blocks). These registers are arranged in a hierarchical configuration along the data flow path between the on-chip memory and processing units within the PE array.